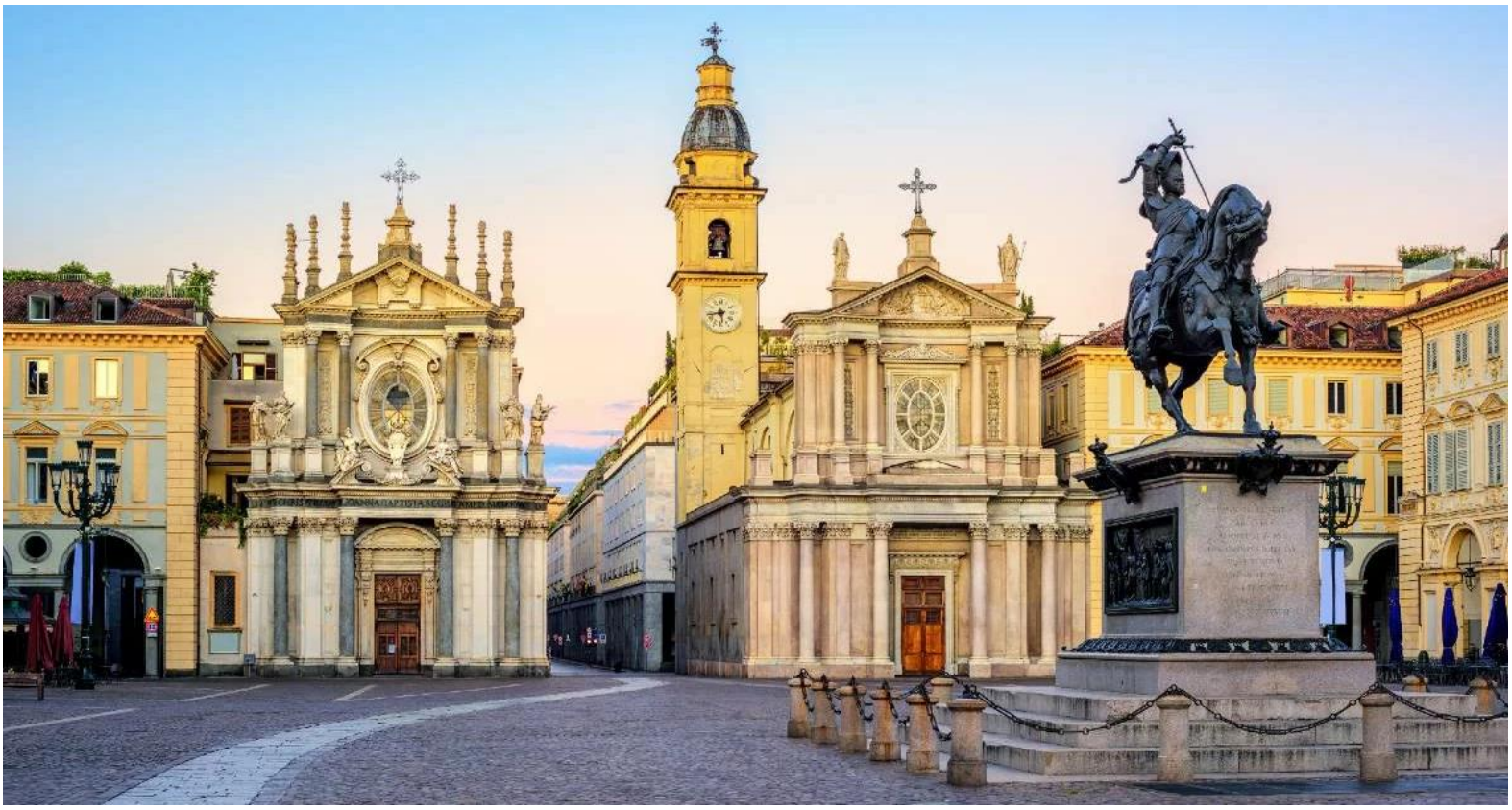


EMC COMPO 2024

October 7th-9th, 2024

Politecnico di Torino

Torino, Italy

The 14th International Workshop on the Electromagnetic Compatibility of Integrated Circuits

Preliminary Program

As of August 12, 2024

Politecnico di Torino

Department of Electronics and Telecommunications

IEEE Advancing Technology for Humanity

EMC SOCIETY

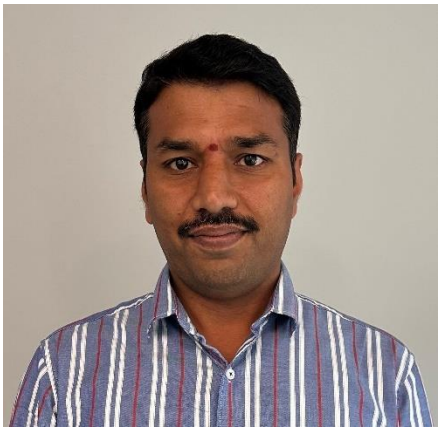
PROGRAM AT A GLANCE

From-To		Monday, 7 October	Tuesday, 8 October	Wednesday, 9 October
9:00	9:30	Welcome ceremony	Invited talk #1: OpAmps highly immune to EMI	Invited talk #2: CM noise reduction in DC-DC converters
9:30	10:00			
10:00	10:30	Coffee break	Coffee break	Coffee break
10:30	11:00	TS#1: Susceptibility to EMI of analog and mixed signals ICs	TS#4: EMC-aware Design of ICs and Guidelines	TS#6: Power Electronics EMC
11:00	11:30			
11:30	12:00			
12:00	12:30			
12:30	13:00	Lunch break and Posters	Lunch break and Posters	Lunch break and Posters
13:00	13:30	Tutorial #1	Tutorial #2	
13:30	14:00			
14:00	14:30			TS #7: SI and PI at IC and PCB level
14:30	15:00	TS #2: Measurement methods for chip level EMC	TS #5: Susceptibility of ICs to Intentional EMI and ESD	
15:00	15:30			
15:30	16:00			
16:00	16:30			
16:30	16:50	Coffee break	Social tour	Coffee break
16:50	17:30	TS #3: Modeling for IC EMC		TS #8: Security and Reliability issues of ICs
17:30	18:00			
18:00	18:30			
18:30	19:00			
19:00	19:30		Gala dinner	
19:30	20:00			
20:00	20:30			
20:30	21:00			
21:00	21:30			

Registration desk opens on Monday 7 at 8:00.

INVITED TALKS

#1: MODELLING AND DESIGN OF HIGHLY EMI IMMUNE CMOS OPAMP TOPOLOGIES



PRESENTER **DR. SUBRAHMANYAM BOYAPATI**
SYNOPSIS, IRELAND

WHEN TUESDAY, 8 OCTOBER 9:10-10:00

ABSTRACT

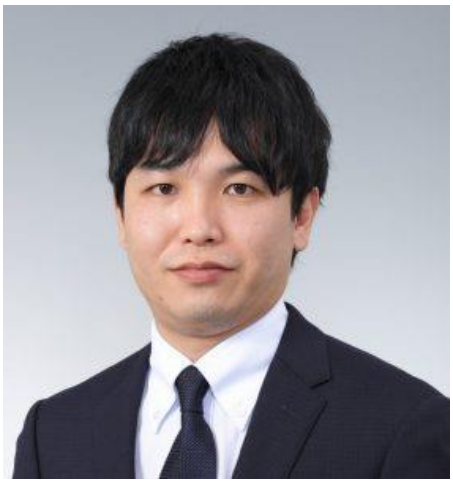
This paper gives a review of the modeling and design of CMOS Miller operational amplifier (OpAmp) and folded cascode operational amplifier that has high immunity to electro-magnetic interference (EMI). The highly EMI immune CMOS OpAmps and folded cascode OpAmps has unique features, such as compact power and low output offset voltage, when compared to the classical Miller OpAmp and the classical folded cascode OpAmps in the literature. The output offset current modeling equations are derived for the CMOS OpAmps including the body effect and channel length modulation. The CMOS OpAmps uses the replica concept along with the source-buffered technique in order to achieve high EMI immunity across a wide range of frequencies (10 MHz to 1 GHz). The highly EMI immune CMOS OpAmps are designed using the first-order quadratic mathematical model. The circuit has been fabricated/designed using 0.18 µm mixed-mode CMOS technology. The performance result shows that the maximum EMI-induced input offset voltage for the CMOS OpAmps is less than 5 mV over a wide frequency range from 1 MHz to 1 GHz, which is lower when compared to the available classical Miller OpAmps and the folded cascode OpAmps.

PRESENTER'S BIOGRAPHY

Subrahmanyam Boyapati received the MTech. degree in integrated electronics and circuits from the Indian Institute of Technology (IIT), Delhi, New Delhi,India, in 2006, and the Ph.D. degree in microelectronics from the IITB-Monash Research Academy, IIT Bombay, Mumbai, India, in 2017. He

is a recipient of the Prime Minister's Fellowship Scheme for Doctoral Research, a public–private partnership between the Science and Engineering Research Board, Department of Science and Technology, Government of India, and Confederation of Indian Industry. From 2018 to 2021, he was an Analog Design Engineer with Intel-Bangalore where he worked on high-speed receiver design for High Bandwidth Memory (HBM) applications. From 2001 to May 2024, he was a Key Researcher with the Center for Integrated Systems and Circuits Design, Carinthia University of Applied Sciences, Austria. Currently he is working as a Senior Staff Analog Design Engineer with Synopsys, Dublin, Ireland. His current research interests include analog and mixed signal integrated circuit design for sensor and biomedical applications, integrated circuit design with a high robustness to electromagnetic interference and high-speed receiver design circuits for the ADCs.

#2: COMMON MODE NOISE REDUCTION METHODS USED FOR HIGH POWER DENSITY DC/DC CONVERTERS



PRESENTER **PROF. JUN IMAOKA**
NAGOYA UNIVERSITY, JAPAN

WHEN WEDNESDAY, 9 OCTOBER 9:10-10:00

ABSTRACT

Compound power semiconductor devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), are widely adapted into automotive, renewable energy, and energy management applications to achieve carbon neutrality. These devices can operate at higher frequencies compared to Silicon (Si)-based devices due to their high switching speed and low on-resistance. Furthermore, high-frequency operation contributes to the realization of high power density in DC/DC converters. However, with the widespread application of compound semiconductor devices capable of high-frequency operation, the importance of common mode noise reduction is significantly increasing. Therefore, this paper introduces state-of-the-art technologies for common-mode noise reduction based on a literature review. Primarily, this paper presents methods for common mode noise reduction in high-power and high-frequency applications without increasing the converter's volume.

PRESENTER'S BIOGRAPHY

JUN IMAOKA (Member, IEEE) received the M.S. and Ph.D. degrees in electronic function and system engineering from Shimane University, Matsue, Japan, in 2013 and 2015, respectively. From October 2015 to March 2018, he was an Assistant Professor with Kyushu University, Fukuoka, Japan. From April 2018 to March 2021, he was an Assistant Professor with Nagoya University, Nagoya, Japan. He is currently an Associate Professor with the Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University. His research interests include the design of integrated magnetic components, modeling for high-power-density power converters, thermal management for power converters, magnetic material application, and EMI of switching power supply.

TUTORIALS

#1 IEC STANDARDIZED IC EMC TEST METHODS: APPLICATION GUIDANCE

PRESENTER **DR. FRANK KLOTZ**
INFINEON TECHNOLOGIES - GERMANY

WHEN MONDAY, 8 OCTOBER 13:00-14:30

ABSTRACT

The tutorial provides in the first part an overview of the current IEC EMC standards for integrated circuits, informs about ongoing and planned standardization projects and gives an outlook on the IC EMC standardization roadmap also with reference to relevant standardization activities in the automotive area at ISO and CISPR. The second part presents and discusses the approach and application of selected IC EMC measurement methods according to the Generic IC EMC Test Specification of the ZVEI.

PRESENTER'S BIOGRAPHY

Frank Klotz, studied electrical engineering at the Technical University of Ilmenau, where he received his PhD in the field of EMC of power semiconductor topologies. In 1996 he started his career in the

semiconductor division of Siemens AG, now Infineon Technologies AG. Today he is head of Infineon's EMC organization, chair of IEC SC47A Integrated Circuits and member of the EMC standardization committees at IEC, CISPR and ISO.

#2 HOW SIGNAL AND POWER INTEGRITY INFLUENCE THE SILICON DEVICE INTEGRATION IN THE PACKAGE AND SYSTEM

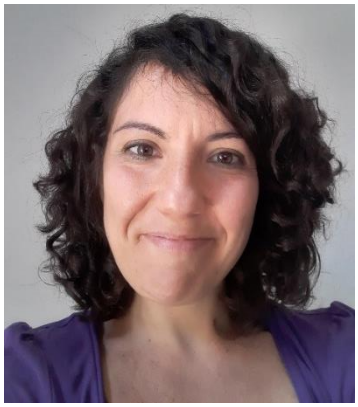
PRESENTERS

OLIVIER BAYET

STMICROELECTRONICS GRENOBLE, FRANCE

AURORA SANNA

STMICROELECTRONICS AGRATE BRIANZA, ITALY



WHEN TUESDAY, 9 OCTOBER 13:00-14:30

ABSTRACT

In the context of integrated circuits development, signal and power integrity (SI & PI) optimization is key to ensure the required electrical performances. With the increasing operating frequencies, decreasing voltage levels and increasing power consumption, package interconnections assume a significant weight and the interaction between chip, package and board needs a deep assessment through a co-design and co-simulation approach. The proposed tutorial goes through the overall design process to optimize signal and power integrity, from pre-layout strategy definition to post-layout verification, with a strong focus on package interconnections technology and design. The importance of chip-package co-design is underlined and a constant link between design, electromagnetic modeling and simulations is maintained, to validate each step of the process.

Main topics:

- Pre-layout strategy for SI and PI optimization
- Die-package-board integration constraints

- Package technology selection based on physical and electrical constraints
- Package routing strategy definition with the support of simulation
- Design partitioning, smart routing strategy definition based on layout symmetries
- Layout optimization and verification for SI and PI
- Signal integrity simulations, from package-level to system-level (frequency-domain and time-domain, input models requirements)
- Power integrity simulations, from package-level to system-level (DC and AC, frequency domain and time-domain, input models requirements, decoupling capacitors selection)
- Link between SI, PI and thermal for accurate analysis
- Link between SI/PI and electromagnetic emissions
- Output chip/package models

PRESENTERS' BIOGRAPHY

Olivier Bayet is Senior Member of Technical Staff at STMicroelectronics and has over 24 years of experience in design and EDA for IC and package. He developed new methods for voltage drop analysis, IC-package co-design and its associated physical and electrical verification. As part of the mobile platform and later networking processor design teams, Olivier setups the design and verification process for SoC-Package-PCB co-design to enable complex interfaces such as LPDDR, DDR, SerDes. Currently Olivier is leading the die/package co-design for various types of projects in the RF & Communication division of ST covering the signal integrity analysis of RF links, antennas, high speed serial links and the system power integrity analysis of low voltage and high-power consumption devices. Olivier holds an MSEE from ENSERB, Bordeaux, France.

Aurora Sanna got the master's degree in Electronics Engineering at Politecnico di Milano, in 2011. Since then, she has worked in the field of electrical modeling of interconnections, starting from PCBs and then moving to IC-packages, dealing with Signal Integrity, Power Integrity and Electromagnetic Compatibility problems. Currently, she is part of Back-end Manufacturing and Technology RnD group in STMicroelectronics and she is leader of a team dedicated to package design, electrical modeling and thermal modeling. She is member of STMicroelectronics Technical Staff.

TECHNICAL SESSIONS

TS#1: SUSCEPTIBILITY TO EMI OF ANALOG AND MIXED SIGNALS ICS

WHEN: MONDAY, 7 OCTOBER 10:30-12:30

Paper ID: #40 10:30-10:50

Characterisation of an EMI-Improved Integrated Folded Cascode Amplifier Structure Using the EMIRR Measurement Method

Author(s): Dominik Zupan, Nikolaus Czepl and Bernd Deutschmann (Graz University of Technology, Austria)

In this paper, we analyse the robustness of operational amplifiers (OpAmps) against electromagnetic interference (EMI). Therefore we compare a standard folded cascode amplifier structure with an EMI-improved amplifier structure introducing a cross-coupled double differential input pair. We perform measurements on the manufactured test chip structures to determine general characteristics (gain, offset, gain-bandwidth product (GBWP) and phase margin), as well as EMI-related characteristics (EMI-induced offset respectively electromagnetic interference rejection ratio (EMIRR)). Based on these characteristics, we compare both structures with regard to their performance. Further on, we put the measurements into relation with our previous findings that we obtained from simulation.

Paper ID: #10 10:50-11:10

Analysis of Operational Amplifier Susceptibility to Multifrequency Disturbance

Author(s): Alexandre Boyer (LAAS-CNRS, France); Fabrice Caignet (LAAS-CNRS & University of Toulouse, France)

This paper deals with the susceptibility of operational amplifiers (op-amps) in multifrequency injection. After an in-depth analysis of the different failure mechanisms that induces DC-offset based on experimental results on a general-purpose op-amp, the paper proposes a risk assessment method based on continuous wave susceptibility test results.

Paper ID: #26 11:10-11:30

Analyzing and Modeling of the Susceptibility to Temporary Malfunction in Automatic Gain Control Loops

Author(s): Tom Billaux (University of Montpellier, IES, France); Jérémy Raoult (Université Montpellier 2, France); Patrick Hoffmann (CEA, France)

The paper presents a study of the dynamic response of an Automatic Gain Control (AGC) loop exposed to a pulsed radiofrequency intentional interference. The influence of the various parameters of the pulse on its behavior is investigated, and a comprehensive model replicating the observed effects is presented. It is demonstrated that the pulse duration optimizing the susceptibility studied here is directly linked to the settling time of the AGC.

Paper ID: #9 11:30-11:50

EMI Immunity of the Nauta Inverter-Based Amplifier

Author(s): Andrea Rosa, Anna Richelli and Luigi Colalongo (University of Brescia, Italy)

This paper investigates the effect of Electromagnetic Interferences (EMI) on inverter-based analog amplifiers, as the Nauta operational transconductance amplifier (OTA). We show that, thanks to the their simple circuital topology that does not include current mirrors and differential pair, the inverter-based analog amplifiers have a much higher EMI immunity: about one order of magnitude.

Paper ID: #11 11:50-12:10

System-On-Chip Preventing Discharge of Bootstrap Capacitor of High-Side Drivers

Author(s): Kamel Abouda (Emc Ic Expert, USA); Matthew Bacchi (NXP Semiconductors Toulouse, France)

Integrated high-side switches are omnipresent in automotive integrated circuits (airbags, power control units, alternator regulators, window lift applications, injectors control…). In non-SOI technologies, parasitic NPN and PNP transistors can degrade IC performance especially when EMC or ESD disturbances are applied to the circuit. This paper presents a small system on chip solution providing remarkably high EMC/ESD susceptibility performance for high-side switch drivers while increasing IC performance during normal operation using a wide range of external components.

Paper ID: #33 12:10-12:30

Evaluation of Ground Terminal Against Noise by Direct Power Injection Method

Author(s): Takashi Nomura (DENSO, Japan); Mitsuhiro Hasegawa and Ko Oyama (Denso Corporation, Japan); Yosuke Kondo (DENSO Corporation, Japan); Koji Ichikawa (Nagoya Institute of Technology, Japan)

This paper shows that the immunity characteristics of integrated circuits (ICs) having a large number of terminals to be evaluated can be evaluated macroscopically by measuring the strength against the noise of the ground terminal. A voltage reference circuit was fabricated in silicon-on-insulator Bipolar / CMOS / LDMOS (SOI-BCD) process [8], and the strength against the noise of power supply terminals and the ground terminal were compared. The strength was measured by direct power injection (DPI) method [1] at each terminal. The reference potential for applying noise to the ground terminal was a potential in a no element region where separated from the circuit region by an insulator. As a result, it was confirmed that the strength against the noise of the ground terminal was same with the low strength of other terminals. In addition, similar results were obtained by a simulation.

TS#2: MEASUREMENT METHODS FOR CHIP LEVEL EMC

WHEN: MONDAY, 7 OCTOBER 14:30-16:30

Paper ID: #34 14:30-14:50

Butterfly Probes: Estimating the Derivative of the Magnetic Flux

Author(s): Philippe Maurine (LIRMM, Montpellier University, France); Jérémy Raoult and Anselme Mouette (University of Montpellier, France); Julien Toulemont (ANSSI, France)

The main way to increase the spatial selectivity of near field probes has been to make coils with smaller and smaller diameters. This is especially true for secure applications (side-channel attacks). In this paper, we investigate an alternative way with secure applications in mind. It consists in designing probes that measure the spatial derivative of the magnetic flux instead of the flux itself. The paper presents the motivation, the concept and preliminary results obtained with a first prototype.

Paper ID: #35 14:50-15:10

Influence of Sensing Resistor on IC-Level Noise Measurement of DC-DC Converters by 1 Ω Method

Author(s): Hyun Ho Park (The University of Suwon, Korea (South)); Jiseong Kim (KAIST, Korea (South)); Eakhwan Song (Kwangwoon University, Korea (South)); Hongseok Kim (CPS Tech, Inc., Korea (South)); Sangho Cho (LG Electronics Inc., Korea (South))

This paper presents a method for determining the appropriate sensing resistance value when measuring integrated circuit (IC) noise in DC-DC converter ICs using the 1 Ω method as outlined in IEC 61967-4. By modeling the DC-DC converter circuit as an equivalent RLC resonance loop and accounting for the parasitic inductance of the sensing resistor, we established the permissible range for the sensing resistance. Through circuit simulations, this study examines the impact of sensing resistance and parasitic inductance on the ringing noise of DC-DC converter ICs, ultimately determining the optimal resistance value for accurate IC-level noise measurement.

Paper ID: #27 15:10-15:30

Near Field Scan Investigation Method to Reduce 4.8GHz Emission on a BLE Application

Author(s): Jeremy Ruau, Bertrand Vrignon and Christophe Menard (NXP Semiconductors, France); Lucy Liu (NXP Semiconductors, China); Matthieu Baudry (NXP Semiconductors, France)

The product studied is a low-power, highly secure, single-chip wireless MCU that integrates high-performance Bluetooth Low Energy for Automotive and Industrial applications. During EMC radiated emission test, a peak appeared around 4.8 GHz, due to 2nd harmonic of BLE. EMC lab proposed new investigation method based on near field scan to analyse the peak and try to improve the emission level. This work aims to first understand the origin of the 4.8GHz peak encounter in RE measurement, then to explain the importance of a good antenna matching network at high frequency and finally to detail the solution found to reduce the emission level.

Paper ID: #28 15:30-15:50

Design and Application of RFIC Detector: To Measure Coupled Power Into IC Pin via PCB Trace

Author(s): Arunkumar Hunasanahalli Venkateshaiah, John F Dawson, Martin Trefzer, Simon Bale, Andy Marvin and Martin Robinson (University of York, United Kingdom (Great Britain))

In this paper, we discuss the design of an RF IC detector with eight channels connected to the package pins, designed to determine the incident RF power on each pin. Some of these channels possess different sensitivity levels based on the amplification circuit block they use. A PCB test bench with test tracks has been designed to allow the measurement of RF power coupled to the detector IC pins when illuminated by a RF source. Our discussion will also encompass the applications of the RF IC detector in detecting stochastic EM fields in reverberant or equivalent real-world environments. The key contribution in this paper is the design of RF IC detector which has these applications.

Paper ID: #17 15:50-16:10

On-Chip ESD Current Sensor for Nanosecond Oscillation Waveform Over Ampere Detecting

Author(s): Kazuki Shimada (Renesas Electronics Corporation, Japan); Mototsugu Okushima (Industry of ESD & Renesas Electronics Corporation, Japan)

To analyze IC destruction and malfunction due to ESD (IEC61000-4-2), we proposed an on-chip current sensor that can accurately capture the entire ESD current waveform flowing into the IC that oscillates significantly for positive and negative in the nanosecond range. Measurement accuracy has improved by compensating for measurement errors caused by voltage overshoot in the nanosecond range of the current detection device. The ESD current waveform flowing into the IC is different from the standardization waveform, and a positive and negative oscillation waveform can come in, and we have designed to handle these polarities. This sensor sets a design window that does not incorrectly respond against noise that does not affect the system, and it only captures ESD currents of ampere or more. This sensor will become an important component for analyzing IC destruction and malfunction due to ESD.

Paper ID: #50 16:10-16:30

Accelerated Characterisation of Operational Amplifiers' Susceptibility Using Multitone Disturbance

Author(s): Matthieu Laidet (LAAS CNRS & EDF Power Network Lab, France); Alexandre Boyer (LAAS-CNRS, France); Sonia Ben Dhia (INSA de Toulouse, France); Julien Gazave (EDF Group, France)

This paper presents an original approach to accelerate susceptibility testing of Operational Amplifiers (op-amp), using large band multitone signals, for a Direct Power Injection (DPI) setup. The relation between Continuous Wave (CW) and multitone susceptibility results, the associated limits and the global characterisation flow are discussed.

TS#3: MODELING FOR IC EMC

WHEN: MONDAY, 7 OCTOBER 16:50-18:50

Paper ID: #47 16:50-17:10

Inspection Tools for Gaussian Process Regression Modeling of Electromagnetic Fields of Electronic Boards and Chips

Author(s): Tomas Monopoli, Xinglong Wu and Sergio A Pignari (Politecnico di Milano, Italy); Karl-Friedrich J Wolf (European Space Agency (ESA) & ESTEC, The Netherlands); Flavia Grassi (Politecnico di Milano, Italy)

Gaussian Process Regression (GPR) has emerged as a powerful technique for building surrogate models of electromagnetic field scans in electronic systems. However, standard GPR models often struggle to capture the non-isotropic and complex spatial patterns commonly found in electronic board field distributions. In this paper, we propose some inspection tools to analyze the underlying correlation structure in the measurement data. This analysis is demonstrated by considering as input data the near field emissions from a bent miscrostrip line (full-wave simulations) and a chip (near-field measurements).

Paper ID: #12 17:10-17:30

An ICIM-CI Model for Mass Production Development Considering Manufacturing Variations

Author(s): Hidetake Sugo (DENSO CORP., Japan); Norimasa Oka (DENSO COPR., Japan); Takaya Nagai, Koji Hattori and Takeshi Matsuzaki (DENSO CORP., Japan)

An ICIM-CI model of an analog circuit with a differential amplification for mass production development is proposed. It is observed that manufacturing variations, such as in terms of the oscillation frequency, cause differences in failure thresholds, obtained by the DPI method, between samples. The maximum difference is 8.7 dB at 1.0 MHz. To predict the lowest forward power that causes failure, a prediction formula based on design information is obtained. By comparing the prediction results with measurements, it is confirmed that the forward power can be estimated within the range of variations.

Paper ID: #39 17:30-17:50

A Case Study for the EMC Co-Simulation of Injection Path Model Using WR Method

Author(s): Md Moktarul Alam (ESEO, France & Institut National Des Sciences Appliquées de Rennes, France); Richard Perdriau and Mohamed Ramdani (ESEO, France); Mohsen Koohestani (ESEO School of Engineering & IETR, University of Rennes, France)

This article highlights an assessment of the co- simulation suitability to evaluate the conducted electromagnetic immunity of an injection path model between source and load circuits using waveform relaxation (WR). The latter enhances co-simulation performance and stability by adjusting the impedance approximation parameter variables with the voltage and current control sources. Additionally, this paper emphasizes the significance of parameter initialization

for interfacing subsystem 1 to 2. Testing is conducted on an injection path model circuit with an input pulse voltage source from 0 to 2.5 V . A comparative analysis with the WR method indicates output voltage difference of less than 1.4% between the full system values after three iterations only. These results highlight the proposed method's ability to achieve faster and more accurate convergence compared to the traditional WR methods.

Paper ID: #24 17:50-18:10

A Simulation Workflow for Predicting IC Stripline Radiated Emissions of Bond Wire-Based Systems

Author(s): Dominik Kreindl (Ams-OSRAM AG & Graz University of Technology, Austria); Bernhard Weiss and Christian Stockreiter (Ams-OSRAM AG, Austria); Thomas Bauernfeind and Manfred Kaltenbacher (Graz University of Technology, Austria)

Light sources in optical sensor packages can cause high levels of electromagnetic interference due to their high current consumption and short switching times. The radiating structures are electrically short for the frequency range of interest for metrological verification according to the IEC 61967-8 standard. This can be used to find an equivalent representation of the emission sources in terms of Hertzian dipole moments. This paper presents a purely analytical simulation workflow for predicting radiated emissions in IC stripline measurements by employing dipole moments. The procedure is evaluated against finite element simulations and measurement data. The results show promising correlations in the lower frequency range, but significant deviations are observed above 1.5 GHz. Further research is needed to identify the root cause of these deviations.

Paper ID: #30 18:10-18:30

Enhancing High-Speed Ethernet Link Design at 25 Gbps in Aerospace Environments Through Optimization Algorithms

Author(s): Soazig Le Bihan (Thales & Laboratoire IMS, France); Tristan Dubois (Laboratoire IMS, France); Jean-Baptiste Begueret (University of Bordeaux I, France); ADIL El Abbazi (Thales AVS, France)

Introducing a new high-speed design requires a careful optimization of any discontinuities that may degrade signal quality. A high-speed signal includes structures such as BGA (Ball Grid Array), vias, AC coupling capacitors, or connectors. Poorly matched impedance may result in undesirable signal reflections, energy losses, and electromagnetic interference. These structures need to be wisely optimized in order to limit signal reflections along the path while taking into account manufacturing constraints, costs, performance and routing density for aerospace products. However, with every change to the design and for each new product, this time-consuming process needs to be evaluated again. This optimization process should be automated and analyzed by algorithms and metamodels in order to reduce analysis time while maintaining simulation accuracy.

Paper ID: #21 18:30-18:50

High-Fidelity S-Parameter Prediction Using Transfer Learning Based Encoder-Decoder Model

Author(s): Ruiqi Dai, Yuhao Xu, Jiarui Qiu, Hanzhi Ma and Er-Ping Li (Zhejiang University, China)

The demand for large-scale data samples has always been a significant bottleneck in the application of artificial intelligence methods in the field of electromagnetic compatibility (EMC) of integrated circuit (IC). This paper proposes the Transfer Learning Encoder-Decoder network (TL-ED) method for predicting circuit S-parameters. Considering the high computational cost involved in obtaining accurate high-fidelity data samples, this method utilizes transfer learning to transfer the rough model, which is modeled based on low-fidelity data with low computational costs, to the accurate model. Subsequently, the model is fine-tuned using a small amount of high-fidelity data. Application results confirm that this approach significantly reduces the demand for high-fidelity data and has the potential to be applied in IC-EMC analysis where data acquisition through testing experiments is necessary.

TS#4: EMC-AWARE DESIGN OF ICS AND GUIDELINES

WHEN: TUESDAY, 8 OCTOBER 10:30-12:30

Paper ID: #63 10:30-10:50

EMI Robust Comparator Design for Protection Features of Smart Power Switches

Author(s): Daniel Kircher (Graz University of Technology, Austria); Cristian Ionascu (Infineon Technologies Austria AG, Austria); Bernd Deutschmann (Graz University of Technology, Austria)

In the field of automotive smart power switches, the integrity of the chip's temperature signal processing and overtemperature recognition are critical. This paper presents a robust input stage for a comparator designed to withstand electromagnetic interference (EMI) while maintaining accuracy. We present a novel design that incorporates hysteresis and uses linearisation techniques to enhance immunity to radio frequency (RF) interference. Our results show a significant improvement in the electromagnetic immunity of the overtemperature protection mechanism. We validate our results with direct power injection (DPI) simulations comparing the standard input topology with the EMI improved one.

Paper ID: #25 10:50-11:10

STT-MRAM Based ESD and EFT Immunity Analysis

Author(s): Jianfei Wu (National University of Defense Technology, China); Yanfang Lu, Yang Li and Hongli Zhang (Tianjin Institute of Advanced Technology, China); Yiming Zhang (Hebei University of Technology, China); Xing Zhao (Institute of Microelectronics of Chinese Academy of Sciences, China); Wei Zhu (Research Institute of Integrated Circuits and Systems Application, China)

This study analyses the Electromagnetic Immunity (EMI) of STT-MRAM. By exhaustively exploring and verifying the Electrostatic discharge (ESD) and Electrical Fast Transient (EFT) of STT-MRAM, the impact of ESD and EFT on the performance of STT-MRAM is investigated, the potential threat of transient electromagnetic interference to STT-MRAM memory is revealed, and suggestions are made to improve its electromagnetic compatibility (EMC), which provides an important reference for its reliable application.

Paper ID: #41 11:10-11:30

Comprehensive Study of EMI Effects on Wireline Transceiver Systems: A Review of Silicon-Proven Techniques

Author(s): Mohit Singh Choudhary (Indian Institute of Technology, Bombay, India); Jean-Michel Redouté (University of Liège, Belgium); Maryam Shojaei Baghini (Indian Institute of Technology, Bombay)

This research paper provides an extensive examination of electromagnetic interference (EMI) in wireline transceiver systems. Wireline transceiver circuits are particularly susceptible to undesired electromagnetic waves in their environment. The paper delves into a mathematical approach for incorporating EMI into circuit simulation tools. Additionally, it explores the impact of EMI on different wireline communication systems, such as LVDS, CML, and PAM-4 transceiver systems. The goal is to comprehensively understand how EMI affects the performance of these wireline communication systems.

Paper ID: #49 11:30-11:50

Evaluation of the Electromagnetic Emission of ICs Using Different Spread Spectrum Approaches

Author(s): Marco Pfeifer, Ko Odreitz and Bernd Deutschmann (Graz University of Technology, Austria)

This paper examines the use of spread spectrum clocking approaches to reduce the increasing electromagnetic emissions caused by the constantly rising switching frequencies of modern electronic systems. The approach to reducing these emissions is based on spreading the spectral power of a narrowband signal over a certain bandwidth in order to reduce the peak amplitude. We will compare the performance of a spread spectrum clock generator (SSCG) based on the random method with one using simple frequency modulation with a triangular modulation signal and relate it to their theoretical behavior. Furthermore, we will perform CISPR-compliant emission measurements with different detectors of an EMI receiver and compare the influence on the measurement results.

Paper ID: #14 11:50-12:10

Effects of Ionizing Radiation on the EMI-Induced Offset Voltage of Operational Amplifiers

Author(s): Nikolaus Czepl, Dominik Zupan, Alicja Michalowska-Forsyth and Bernd Deutschmann (Graz University of Technology, Austria)

In this work, we investigate the impact of ionising radiation on the robustnes towards electromagnetic interference (EMI) of operational amplifiers (OpAmps). Therefore we irradiate two OpAmps, one including a standard differential input stage structure, the other OpAmp featuring a second crosscoupled double differential input pair added to the standard input stage structure. We perform measurements on the manufactured test chip structures to determine

general characteristics (gain, offset, gain-bandwidth product (GBWP) and phase margin), as well as EMI-related characteristics like EMI-induced offset and electromagnetic interference rejection ratio (EMIRR). Based on these characteristics, we compare both structures with regard to their performance prior to, during and after irradiation with X-rays. We observe a change in the EMIRR performance with increasing ionising dose. Finally, we explain our observations by taking into account transistor-level effects.

Paper ID: #57 12:10-12:30

Accuracy of GPS Positioning Measurements in Response to Electromagnetic Noise Characteristics

Author(s): Hiraku Uehara (Kobe University, Japan); Koh Watanabe (National Institute of Information and Communications Technology, Japan); Sosuke Ashida, Yushi Mitsuya, Satoshi Tanaka and Makoto Nagata (Kobe University, Japan)

Autonomous vehicles, such as unmanned aerial vehicles (UAV) and self-driving cars, have been recently used deployed. Many of them use a global positioning system (GPS) to acquire location data, which requires high accuracy. On the other hand, the electromagnetic (EM) environment inside the autonomous vehicle is prone to electromagnetic interference (EMI) between EM noise and GPS signals, and there is a risk that this EMI inside the autonomous vehicle may deteriorate the accuracy of GPS positioning measurements. Previous studies have reported the interference of EM noise from UAVs with global navigation satellite system (GNSS) and with mobile communications. Evaluations and countermeasures for the EMI problems are necessary since the low accuracy of positioning measurements may lead to malfunctions and accidents. This study showed the accuracy of positioning measurements under two EM noise components, which are experimented with the EMI of EM noise to GPS signal with a GPS receiver module. As a result, we found that the characteristics of EMI were dependent on EM noise components, specifically, random noise and harmonic noise.

TS#5: SUSCEPTIBILITY OF ICS TO INTENTIONAL EMI AND ESD

WHEN: TUESDAY, 8 OCTOBER 14:30-16:30

Paper ID: #29 14:30-14:50

Assessing IEMI Vulnerabilities in MEMS Barometers: A Comparative Approach

Author(s): Louis Cesbron Lavau (RWTH Aachen & Fraunhofer INT, Germany); Michael Suhrke (Fraunhofer INT, Germany); Peter Knott (Fraunhofer FHR, Germany)

As the Internet of Things (IoT) expands, sensors play a crucial role in collecting and transmitting vital data across various domains. However, their susceptibility to Intentional Electromagnetic Interference (IEMI) raises significant concerns. This paper investigates the vulnerabilities of barometric sensors to IEMI. Utilizing a methodology similar to previous studies, measurements were conducted using Continuous Wave (CW) and pulse signals to assess sensor behavior under IEMI. The findings reveal differences in susceptibility between the studied barometers highlighting distinct vulnerabilities and responses to electromagnetic interference. Specifically, variations in temperature and pressure readings, along with system crashes induced by IEMI, were observed. Additionally, potential coupling paths on PCBs are discussed. This study underscores the importance of tailored mitigation strategies for sensor-based systems.

Paper ID: #16 14:50-15:10

Susceptibility of an Analog Temperature Measurement Function: First Step to Optimize the IEMI Waveform

Author(s): Antoine Duguet (University of Bordeaux & Thales SIX, France); Tristan Dubois (IMS BORDEAUX, France); Genevieve Duchamp (IMS, France); David Hardy and Franck Salvador (Thales SIX, France)

This contribution deals with the electromagnetic susceptibility of an electronic function based on the susceptibility of its components. The susceptibility of the electronic function has been measured and modelized from its component's susceptibility characterizations. The function has been submitted to some modulated interferences to observe their susceptibility behaviors and vulnerabilities.

Paper ID: #62 15:10-15:30

Controlling Faulty Byte Outputs With IEMI Against Cryptographic ICs

Author(s): Hikaru Nishiyama (National Institute of Advanced Industrial Science and Technology (AIST) & Nara Institute of Science and Technology (NAIST), Japan); Daisuke Fujimoto and Yuichi Hayashi (Nara Institute of Science and Technology, Japan)

Intentional electromagnetic interference (IEMI) for cryptographic integrated circuit (IC) has been reported as a threat for fault injection attack that extracts secret key information by inducing temporary fault in a specific number of bytes in the cryptographic process. And the previous studies on IEMI fault injection have focused on whether it is possible to generate only 1-byte fault, which is necessary for Piret's Differential Fault Analysis (DFA), a secret key analysis method. On the other hand, some methods have been proposed that use multiple-byte faults to enable secret key analysis even under attack conditions where DFA is difficult to apply. If multiple-byte faults that are applicable to such analysis methods can be generated, the threat of IEMI fault injection may increase. In this paper, we show that the number of faulty bytes can be precisely controlled by varying the parameter of the EM waves injected to the cryptographic IC with high resolution, and that the faults output by IEMI fault injection can be used for analysis methods other than DFA. Specifically, we use impulses as the EM waves, measure the electrical changes that occur in the cryptographic IC when the amplitude and pulse width are manipulated, and investigate the relationship between the number of faulty bytes and the electrical changes.

Paper ID: #67 15:30-15:50

Modeling and Analysis of On-Chip Voltage Fluctuations Caused by Electromagnetic Fault Injection

Author(s): Takuya Wadatsumi, Rikuu Hasegawa, Kazuki Monta and Takuji Miki (Kobe University, Japan); Lang Lin and Norman Chang (ANSYS, Inc., USA); Makoto Nagata (Kobe University, Japan)

Near-field electromagnetic fault injection (EMFI) is one of the most commonly used attack methods to intentionally cause errors in digital circuits due to its inherent advantages. A full-wave simulator was used to analyze the voltage fluctuations on the on-chip power mesh excited by EMFI. We have described the relationship in which the shape of the voltage fluctuations on the power mesh inside ICs is derived from the differentiation of the current flowing through the

injection coil by using Maxwell's equations and full-wave simulations. In addition, the results with different injection positions and ideal voltage source points have showed that the areas of high sensitivity vary on the power supply mesh.

Paper ID: #55 15:50-16:10

Analysis, Testing and Comparison of Different Commercial ESD Detectors

Author(s): Musab Hameed, Abraham Reithofer and Gabriel Fellner (Graz University of Technology, Austria); Ahmad Hosseinbeig (Apple, USA); David Pommerenke (TU Graz, Austria)

This paper investigates the response of various commercial electrostatic discharge (ESD) detectors with respect to their ability to detect charged device model (CDM) like short pulses and their ability to discriminate between CDM and non-CDM pulses. A series of test setups (TEM cell, sphere-to-Gnd discharge, narrow pulse generator) were set up to evaluate how different detectors behave at different pulse widths and field strengths. Pulse durations varying from 150 ps - 16 ns FWHM were applied in the different test setups. The measured responses of the detectors under different ESD conditions are analyzed and compared.

Paper ID: #44 16:10-16:30

Functional Failures in a Sensor Application Caused by System-Level ESD

Author(s): Stefan Jahn (Infineon Technologies AG, Germany)

This paper reports the functional behavior of a system consisting of a pressure sensor within its sensor module, a two-wire supply with current modulated communication channel and an electronic control unit equivalent during powered system-level ESD tests. It discusses functional recoverable soft-failures, their failure mechanisms and root causes considering overall system properties as well as special electro-mechanical integrated circuit properties, and ESD test requirement and procedures.

TS#6: POWER ELECTRONICS EMC

WHEN: WEDNESDAY, 9 OCTOBER 10:30-12:30

Paper ID: #42 10:30-10:50

Passive DC-Input and DC-Input/AC-Output EMI Filter for DC-AC Inverter

Author(s): Matthias Schulz and Michael Kopf (Siemens AG, Germany)

This paper aims to compare the performance of an electromagnetic interference (EMI) direct current (DC)-input filter with a combined DC-input/alternating current (AC)-output filter. The EMI filters will be implemented in a DC-AC inverter to comply with regulatory standards. The DC-AC inverter has a two-level topology, with a defined switching frequency of 4 kHz. A theoretical model of the entire system, including the considered parasitic elements for cables, DC-AC inverter, and motor, is presented. Single-phase equivalent circuits for common mode (CM) and differential mode (DM)

noises are derived from this circuit. The required attenuation to fulfill the standards for the two-level inverter is used to evaluate the influence of the EMI filter components and necessary filter stages. To accomplish this, the noise spectrum of the two-level topology without any EMI measures and the limit lines of two different regulatory standards are utilized. Considering this perspective, the passive components of the EMI filters are selected, with separate investigations conducted on CM and DM noises. Finally, conducted EMI measurements on a 55 kW DC-AC inverter prototype validate the proposed filter damping. Deviations between measured noise spectrum and the expected damping are discussed in detail.

Paper ID: #60 10:50-11:10

A Comparison of Spread Spectrum and Sigma Delta Modulations to Mitigate Conducted EMI in GaN-Based DC-DC Converters

Author(s): Alberto Barbaro, Markeljan Fishta, Erica Raviola and Franco Fiori (Politecnico di Torino, Italy)

This paper presents a comparison of two modulation schemes, Spread-Spectrum Modulation (SSM) and Sigma-Delta Modulation (ΣΔM), in the context of conducted Electromagnetic Interference (EMI) mitigation in GaN based dc-dc converters. Despite the advantages of GaN power transistors, their adoption poses significant challenges in ensuring the compliance of converters to EMC regulations due to the increased EMI caused by fast switching transients. This study investigates the effectiveness of SSM and ΣΔM, as compared to traditional PWM. The paper provides insights into the effects of these techniques on converter performance and conducted EMI. The findings will serve as a useful guide for designers in determining the most effective strategy for EMI reduction.

Paper ID: #37 11:10-11:30

DM EMI Noise Prediction for BCM Based Single-Phase Grid-Connected Inverter

Author(s): Chen Liu, Freede Blaabjerg and Pooya Davari (Aalborg University, Denmark)

Boundary conduction mode (BCM) can be employed in single-phase grid-connected inverters to enhance the efficiency due to its soft-switching feature. However, high inductor current ripple brings high differential mode electromagnetic interference (EMI) noise. This paper proposes an analytical model to predict the differential mode EMI noise for BCM based single-phase grid-connected inverter, which can facilitate the design of the EMI filter without repetitive measurements. Experimental results of a 500 W prototype are provided to validate the feasibility and effectiveness of the proposed prediction method.

Paper ID: #61 11:30-11:50

A Critical Analysis of Amplifier Requirements in Capacitance-Boosting Circuits for EMI Reduction

Author(s): Markeljan Fishta, Pietro Montorsi and Franco Fiori (Politecnico di Torino, Italy)

This work presents a comprehensive and critical analysis of the amplifier requirements for capacitance-boosting circuits, like those used in active EMI filters. The relationship between the amplifier specifications and the overall performance of these circuits is investigated. The study begins with an overview of the fundamental principles of capacitance-boosting circuits, followed by an in-depth exploration of the role of amplifiers in these systems. Then, various amplifier parameters such as bandwidth, output impedance, and output swing are critically analyzed,

highlighting their impact on the performance of capacitance-boosting circuits. Through rigorous theoretical analysis and computer simulations, this work provides valuable insights into the optimal amplifier requirements for capacitance-boosting circuits.

Paper ID: #69 11:50-12:10

Analysis of Partial RF Emission Spectra of IC Functions and Subcircuits on the Example of Power Switch ICs

Author(s): Sergey Miropolsky and Frank Klotz (Infineon Technologies, Germany)

This paper presents a simulation based approach to decompose the overall conducted RF emission of a complex integrated circuit (IC) into partial emission spectra due to various functional blocks or processes in the analyzed DUT IC. The approach is described based on a generic power switch.

Paper ID: #36 12:10-12:30

Measurement of PCB-Related Commutation-Loop Inductance Using a Vector Network Analyzer

Author(s): Maurizio Tranchero (Ideas & Motion, Italy); Marco Garelli (Keysight Italy Srl, Italy)

The stray inductance in the commutation loop is cause of oscillations that affect the efficiency of a power converter and are source of electromagnetic noise. Since the advent of Wide Band-Gap (WBG) power devices made possible generating steeper current and voltage transition, these high-speed switching is exacerbating the phenomenon. Commercial components are characterized by the manufacturers and datasheets are often reporting the value of the stray inductance for a given package. Unfortunately this is not enough, since the Printed Circuit Board (PCB) introduces the main part of the commutation loop inductance. This paper proposes to use Vector Network Analyzer (VNA) measurements to characterize the impedance of a bare PCB trace. The presented method has proved to be reliable in comparing different PCB designs to determine the best one.

TS#7: SI AND PI AT IC AND PCB LEVEL

WHEN: WEDNESDAY, 9 OCTOBER 14:10-16:30

Paper ID: #46 14:10-14:30

Automated Method to Synthesize RLCK-Circuits From S-Parameters

Author(s): Alexander Schade (Infineon Technologies AG Neubiberg, Germany); Frank Klotz (Infineon Technologies, Germany); Robert Weigel (Friedrich-Alexander Universität Erlangen-Nürnberg, Germany)

To understand and control parasitic elements on the PCB, package and chip level, designers require compact yet precise circuit models. The PEEC methods and "classical" parasitic extraction exhibit distinct disadvantages when applied to

systems comprising layered planar conductors: Due to their reliance on partial inductances, the resulting models are not very intelligible and comparably complex. In contrast, our approach
synthesizes highly compact and interpretable circuits based on loop inductances. Our novel method is more general than the algorithm by YOUNG. At the core of our technique is an exact equivalent circuit of multi-port S-parameters, applicable also to electrically large systems and radiation coupling.

Paper ID: #48 14:30-14:50

Loop Inductance Based RLCK Models of PCBs and IC-Packages in Practice

Author(s): Alexander Schade (Infineon Technologies AG Neubiberg, Germany); Frank Klotz (Infineon Technologies, Germany); Robert Weigel (Friedrich-Alexander Universität Erlangen-Nürnberg, Germany)

Loop inductances offer decisive advantages over partial inductances when electromagnetic systems shall be modeled in a compact and understandable manner. This publication builds on a previously published mathematical technique to extract physical "white-box" models from S-parameters of systems comprising, e.g., power IC metallization, interposers, IC-packages, PCBs and an environment. It is shown how a complex layout can be segmented by means of differential source and sink ports, forming a multigraph. The ports should be arranged in order to minimize the number of large magnetic couplings by reducing loop area and overlap. We discuss microstrips, striplines, vias, half bridges, multiple ground nets and discrete components. Applications range from CMOS SoCs over integrated Automotive ICs and fast-switching DC/DC-converters to high-power modules (SiC MOSFETs, GaN HEMTs).

Paper ID: #64 14:50-15:10

Suppression of Power Distribution Network PCB-Package Resonance for Low Target Impedance

Author(s): Francesco de Paulis (University of L'Aquila, Italy); Faye Squires (Missouri University of Science and Technology, USA); Yifan Ding (Missouri UNiversity of Science and Technology, USA); Matteo Cocchini, Matthew Doyle and Samuel Connor (IBM Corporation, USA); Albert Ruehli (Missouri University of Science and Tech, Jordan); Chulsoon Hwang (Missouri University of Science and Technology, USA); Lijun Jiang (Missouri University of Science and Technology, USA & EMC Lab, USA)

The suppression of the large resonance peak that may appear due to the equivalent parallel circuit between the package capacitance and PCB inductance is discussed. The relevant parameters involved in the PDN design and a feasible solution strategy are presented.

Paper ID: #66 15:10-15:30

Investigation on the Effect of Different Form Factors on the Performance of Miniaturized Transformers

Author(s): Simone Negri, Xiaokang Liu, Giordano Spadacini, Flavia Grassi and Sergio A Pignari (Politecnico di Milano, Italy); Aurora Sanna and Damian Halicki (STMicroelectronics, Italy)

Miniaturized transformers have become essential components to enable the realization of compact, efficient, and cost-effective electronics systems. Depending on the selected substrate and technology, planar micro-transformers can be

integrated directly on a silicon device, included as stand-alone components in a System-in-Package (SiP) approach, or mounted directly on PCB. In this paper, an investigation on the effect of different form factors, defined as the ratio between the shorter and longer substrate sides, on the performance of miniaturized transformers is presented. Relevant performance indicators are defined, and a test case is numerically analysed, varying the form factor from 1 to 0.46, with 0.01 steps. The presented results show marginal variations on both voltage ratio and efficiency for form factors ranging from 1 to 0.8, while potentially severe reduction in efficiency up to 10 % can be expected for form factors smaller than 0.5.

Paper ID: #15 15:30-15:50

Reconfigurable Board-To-Board Interconnect Utilizing Bistable Compliant Ribbon Wires

Author(s): Norbert Seliger (Technische Hochschule Rosenheim, Germany); Nico Leirich (Technical University of Applied Sciences Rosenheim, Germany)

We propose a printed circuit board (PCB) interconnection utilizing elastically deformed ribbon wires. The wire deflection is designed as a bistable snapping mechanism, which enables post-assembly tuning of the geometry. Hence, a reconfigurable inductance is obtained, easing impedance matching and supporting signal integrity. Analytical solutions for partial and mutual inductance of buckled wires are developed, which are successfully validated by magneto-quasistatic field simulations and by experiments on a test structure for frequencies ranging from 100kHz to 100MHz. We demonstrate a tunable loop inductance from 25nH to 50nH at 10MHz.

Paper ID: #23 15:50-16:10

SPICE Based SI-PI Co-Simulation Framework to Optimize Die-Package-PCB to Meet LPDDR5(x) Performance in Automotive and Edge MPU-MCU

Author(s): Pawan Kumar Gupta (NXP Semiconductors India, India); Rohit Halba (NXP Semiconductors & NXP Semiconductors India PVT. LTD., India)

This paper represents SPICE based Signal Integrity (SI) and Power Integrity (PI) co-simulation framework, which would help in accurate modeling as well as optimizing the system-level components including Die, Package and printed circuit board (PCB) to meet the LPDDR5(x) performance. The proposed framework has integrated all the system level components starting from 32-bit (LP)DDR SPICE IO bank, Die redistribution layer (RDL) SPEF (standard parasitic extraction format) for signals & power as a Die component, interconnects modelled as S-parameters, and the DRAM model which has package, RDL interconnect model & IBIS from DRAM vendor. The DDR protocol operates at burst which may also align with the system resonance frequency resulting into significant on-die power ripple, and due to that timing would be impacted. The SoC Power RDL SPEF is required to accurately model die-capacitance (CDIE) & die-resistance (RDIE) so that power distribution network (PDN) resonance peak amplitude & frequency can be tuned to get the on-die ripple & timing within specifications. This paper would also cover the data pattern recommendation in order to capture the impact of power supply induced jitter (PSIJ) and inter-symbol interference (ISI) & crosstalk due to interconnects on timing.

Paper ID: #58 16:10-16:30

Investigations on Microstrip and Ground Plane Inductance for Conducted EMI Modelling

Author(s): Andree Malina Scambor (Graz University of Technology, Austria); Christoph Maier (Graz University of Technology & Christian Doppler Laboratory for Technology Guided Electronic Component Design and Characterisation, Austria)

This work deals with the inductive behaviour of microstrip traces, ground planes and similar structures for the purpose of conducted EMI simulation. PEEC simulations are performed for different pairings of trace-width, ground plane-width and height of trace over the ground plane. The results of the simulations are presented and discussed and show a dependence on skin and proximity effects. A proposed modelling strategy based on the results is presented and verified for a microstrip line and a capacitor. The capacitor is modelled as a sheet current in a certain height over the ground plane, depending on the internal structure of the capacitor.

TS#8: SECURITY AND RELIABILITY ISSUES OF ICS

WHEN: WEDNESDAY, 9 OCTOBER 16:50-18:30

Paper ID: #51 16:50-17:10

Current Consumption Modeling of Logic Cells Based on Measurements for Side-Channel Attack Simulation

Author(s): Daisuke Fujimoto, Taichi Sato and Yuichi Hayashi (Nara Institute of Science and Technology, Japan)

Side-channel attacks, which estimate the internal secret key by analyzing the radiated electromagnetic waves generated by the current consumption of the encryption circuit, represent a realistic threat. To achieve resistance against side-channel attacks, the current consumption of the encryption circuit must be independent of the secret key. In circuit design, side-channel resistance should be evaluated by simulation to reduce rework costs. For this purpose, a highly accurate power model for logic cells is needed to represent the minute differences in power consumption that vary with input during the encryption process. However, in ASIC design and FPGAs, models are provided only to estimate overall power consumption. In this paper, we propose a method to extract the power consumption of a single logic cell with high accuracy from power consumption measurements of multiple same logic cells to avoid background noise, and show that the increase in peak power consumption with the number of elements when NAND logic is implemented is captured linearly. This measurement method archives express the difference in power consumption caused by the different directions of logic transitions.

Paper ID: #19 17:10-17:30

Clock Signal Recovery Algorithm for FPGA-Based Microcontroller Near-Field EMI Measurement and Processing

Author(s): Shih-Yi Yuan, Shih-Hsien Chiang and Yun-Ling Wang (Feng Chia University, Taiwan); Liang-Yang Lin (Bureauof Standards, Metrology & Inspection, Taiwan); Yuan-Fu Ku (Taiwan Testing and Certification Center, Taiwan)

Embedded systems exhibit variability in emitted EMI when executing different instructions. In order to further analyze EMI signals and identify their correlations with the internal behavior of specific DUT (an FPGA-based microcontroller), an improved algorithm for processing clock signals proposed to recover distorted clock waveform. This innovative approach allows for more accurate and stable FPGA-based microcontroller EMI signal segmentation and analysis. This technique can provide technical support for electromagnetic information leakage security analysis in embedded systems.

Paper ID: #65 17:30-17:50

Fundamental Study on Detecting Hardware Trojans in Printed Circuit Boards Using Ring Oscillators

Author(s): Koki Abe, Daisuke Fujimoto and Yuichi Hayashi (Nara Institute of Science and Technology, Japan)

Threats arise when malicious circuits, known as hardware trojans (HT), are inserted into information devices, compromising security. These HTs can be inserted during the design and manufacturing process of devices, and thus, methods to detect them at the time of manufacturing have been studied. In recent years, it has been pointed out that HTs can also be inserted into parts such as printed circuit boards (PCBs) even after shipping, requiring detection throughout the lifetime of the device. To address this threat, sensing methods using analog circuits have been proposed, but their application is limited. In contrast, this paper proposes a method using a ring oscillator (RO), which can be generally implemented with digital circuits, to detect electrical changes caused by the insertion of HTs. Specifically, the wiring of the RO configured inside the IC is extended externally, and the changes in propagation delay caused by HT insertion on the wiring are detected as changes in the oscillation frequency of the RO. As a result of confirming the effectiveness of the proposed method through experiments, it was confirmed that the proposed method can be used to detect capacitance changes even when a small HT consisting of only a single transistor is connected to the wiring on the PCB.

Paper ID: #20 17:50-18:10

Research and Application Progress on Electromagnetic Reliability of Integrated Circuits in the Past Decade

Author(s): Chen Ledong, Jianfei Wu and Changlin Han (National University of Defense Technology, China); Honghai Liu (University of Defense Technology, China); Xuesong Wang (National University of Defense Technology, China)

Based on the research of electromagnetic reliability (EMR) related articles in the past decade, this paper reviews the influencing factors, evaluation methods, and research progress of EMR, and explores possible future technological applications and development trends. Finally, the challenges and future prospects of current EMR research were analyzed.

Paper ID: #38 18:10-18:30

Experimental Evaluation for Detecting Aging Effect on Microcontrollers Based on Side-Channel Analysis

Author(s): Yuki Kaneko (Tohoku University, Japan); Yuichi Hayashi (Nara Institute of Science and Technology, Japan); Naofumi Homma (Tohoku University, Japan)

Electronic devices are in danger of being unsafe or unreliable since counterfeit integrated circuits (ICs) including recycled ones are on the market while a demand for semiconductor devices is increasing. Especially, MOSFETs in recycled ICs have commonly higher threshold voltage and slower switching speed than new ones, then we have a possibility to observe the aging effects of ICs electromagnetic (EM) emission. In this paper, we focus on around fundamental frequency band given by the clock signal fed into microcontroller, where significant side-channel information is commonly observed, and show a set of experiments to measure voltage variations around the fundamental frequency and lower one from new (unaged) ICs and aged ICs. Through the experiments, we confirm the possibility that we can distinguish aged microcontrollers from unaged ones by this method.

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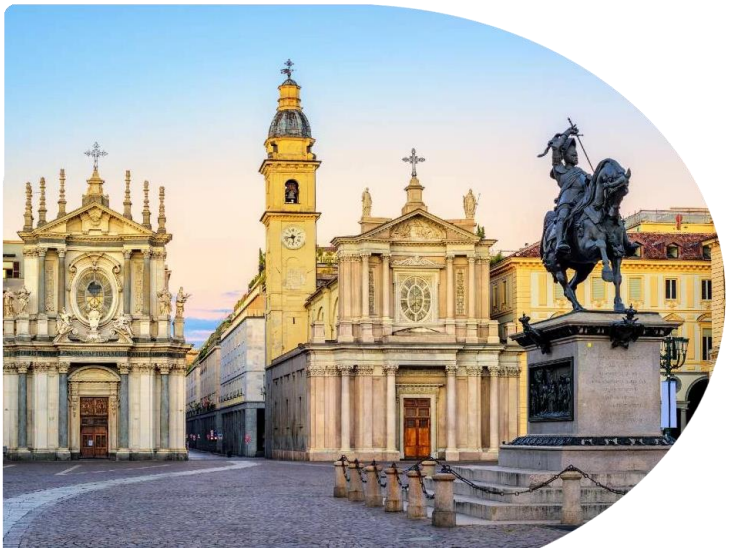

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